CLAIMS

What is claimed is:

1. A register file supplied by a supply voltage V_{dd} and comprising a plurality of threshold voltage V_t bitlines, each of said plurality of V_t bitlines comprising a read-selection transistor having a gate coupled to a dynamic read selection (RS) signal, further comprising a circuit interposed between the RS signal and the gate for increasing a level of a drive signal applied to the gate to be greater than V_{dd}.

2. A register file as in claim 1, where the each of the plurality of V_t bitlines comprise local bitlines (LBLs).

3. A register file as in claim 1, where the read-selection transistor is comprised of a high voltage threshold transistor that is coupled in series with a lower voltage threshold bitcell data transistor.

4. A register file as in claim 1, where the circuit is powered by the supply voltage V_{dd} and is comprised of a driver having an input coupled to the dynamic read selection (RS) signal and an output coupled to a gate of a FET that is coupled in series with a bootstrap capacitance C_B for selectively discharging C_B to increase the level of the drive signal.

5. A register file as in claim 4, where the circuit operates to boost the V_{GS} of the read-selection transistor by an amount delta V (ΔV), where the boost ratio is defined by:

$$\Delta V/V_{dd} = (C_B/(C_B+C_O))*V_{dd},$$

where C_O represents the load capacitance of a read wordline (RWL) coupled to the gate of the read-selection transistor.

6. A register file as in claim 5, where V_{dd} equals about 0.9V, and $V_{dd}+\Delta V$ equals about 1.5V.

7. A register file as in claim 5, where there are a plurality of individually selectable boost circuits having their inputs coupled together in parallel to the dynamic read selection (RS) signal and their outputs coupled together for providing a plurality of selectable boost ratios at the gate of the read-selection transistor.

8. A register file as in claim 1, where the circuit is powered by a supply voltage that is greater than V_{dd} (V_{ddH}) and is comprised of a driver having an input coupled to the dynamic read selection (RS) signal and an output coupled to a gate of a FET, where an output of the circuit is taken from a second driver having an input coupled to an output of the FET.

9. A register file supplied by a supply voltage V_{dd} and comprising a plurality of dual threshold voltage V_t local bitlines (LBLs), each of the dual V_t bitlines comprising a high voltage threshold read-selection transistor (M2) having a gate coupled to a dynamic read selection (RS) signal and coupled in series with a lower voltage threshold bitcell data transistor (M1), further comprising a circuit interposed between the RS signal and the gate of M2 for increasing a level of a drive signal applied to the gate to be greater than V_{dd}.

10. A register file as in claim 9, where the circuit is powered by the supply voltage V_{dd} and is comprised of a driver having an input coupled to the dynamic read selection (RS) signal, and an output coupled to a gate of a FET that is coupled in series with a bootstrap capacitance C_B for selectively discharging C_B to increase the level of the drive signal.

11. A register file as in claim 10, where the circuit operates to boost the V_{GS} of M2 by an amount delta V (ΔV), where the boost ratio is defined by:

$$\Delta V/V_{dd} = (C_B/(C_B+C_O))*V_{dd},$$

where C_O represents the load capacitance of a read wordline (RWL) coupled to the gate of M2.

12. A register file as in claim 11, where V_{dd} equals about 0.9V, and $V_{dd}+\Delta V$ equals about 1.5V.

13. A register file as in claim 10, where there are a plurality of individually selectable boost circuits having their inputs coupled together in parallel to the dynamic read selection (RS) signal and their outputs coupled together for providing a plurality of selectable boost ratios at the gate of M2.

14. A register file as in claim 9, where the circuit is powered by a supply voltage that is greater than V_{dd} (V_{ddH}) and is comprised of a driver having an input coupled to the dynamic read selection (RS) signal and an output coupled to a gate of a FET, where an output of the circuit is taken from a second driver having an input coupled to an output of the FET.

15. In a dual-V_t bitline circuit comprising a high-V_t read-selection transistor and a low-V_t bitcell data transistor, a method to increase the drive current to the high-V_t transistor comprising:

applying a read select (RS) signal; and

boosting the maximum voltage level of the RS signal so that it exceeds the level of the circuit supply voltage V_{dd} before applying the RS signal to the gate of the high-V_t read-selection transistor.

16. A method as in claim 15, where boosting comprises operating a circuit powered by the supply voltage V_{dd} and that is comprised of a driver having an input coupled to the RS signal and an output coupled to a gate of a FET that is coupled in series with a bootstrap capacitance C_B for selectively discharging C_B to increase the level of a drive signal coupled to the gate of the high-V_t read-selection transistor.

17. A method as in claim 16, where the circuit operates to boost the V_{GS} of the high-V_t read-selection transistor by an amount delta V (ΔV), where the boost ratio is defined by:

$$\Delta V/V_{dd} = (C_B/(C_B+C_O))*V_{dd},$$

where C_O represents the load capacitance of a read wordline (RWL) coupled to the gate of the high-V_t read-selection transistor.

18. A method as in claim 17, where V_{dd} equals about 0.9V, and $V_{dd}+\Delta V$ equals about 1.5V.

19. A method as in claim 16, where there are a plurality of individually selectable boost circuits having their inputs coupled together in parallel to RS signal and their outputs coupled together for providing a plurality of selectable boost ratios at the gate of the high-V_t read-selection transistor.

20. A method as in claim 15, where the circuit is powered by a supply voltage that is greater than V_{dd} (V_{ddH}) and is comprised of a driver having an input coupled to RS signal and an output coupled to a gate of a FET, where an output of the circuit is coupled to the gate of the high-V_t read-selection transistor and is taken from a second driver having an input coupled to an output of the FET.

21. A register file supplied by a supply voltage V_{dd} and comprising single threshold voltage V_t bitlines, each of said bitlines comprising a read-selection transistor having a gate coupled to a dynamic read selection (RS) signal, further comprising a circuit interposed between the RS signal and the gate for increasing a level of a drive signal applied to the gate to be greater than V_{dd}.

22. A register file as in claim 21, where the read-selection transistor is comprised of a high voltage threshold transistor that is coupled in series with a high voltage threshold bitcell data transistor.

23. A register file as in claim 21, where the read-selection transistor is comprised of a low voltage threshold transistor that is coupled in series with a low voltage threshold bitcell data transistor.

24. A register file as in claim 21, where the circuit is powered by the supply voltage V_{dd} and is comprised of a driver having an input coupled to the dynamic read selection (RS) signal, and an output coupled to a gate of a FET that is coupled in series with a bootstrap capacitance C_B for

selectively discharging C_B to increase the level of the drive signal.

25. A register file as in claim 24, where the circuit operates to boost the V_{GS} of the read-selection transistor by an amount delta V (ΔV), where the boost ratio is defined by:

$$\Delta V/V_{dd} = (C_B/(C_B+C_O))*V_{dd},$$

where C_O represents the load capacitance of a read wordline (RWL) coupled to the gate of the read-selection transistor.

26. A register file as in claim 25, where V_{dd} equals about 0.9V, and $V_{dd}+\Delta V$ equals about 1.5V.

27. A register file as in claim 25, where there are a plurality of individually selectable boost circuits having their inputs coupled together in parallel to the dynamic read selection (RS) signal and their outputs coupled together for providing a plurality of selectable boost ratios at the gate of the read-selection transistor.

28. A register file as in claim 21, where the circuit is powered by a supply voltage that is greater than V_{dd} (V_{ddH}) and is comprised of a driver having an input coupled to the dynamic read selection (RS) signal and an output coupled to a gate of a FET, where an output of the circuit is taken from a second driver having an input coupled to an output of the FET.